Abstract of the Disclosure

A clock generator generating a refresh clock signal used in a refresh execution of a semiconductor includes a first MOS transistor diode-connected for outputting a first bias voltage, a source of the first MOS transistor being connected to a supply voltage; a second MOS transistor diode-connected for outputting a second bias voltage, a source of the second MOS transistor being connected to ground voltage; a bias current control means having a predetermined number of serial-connected diodes for serving as a resistance in inverse proportion to a temperature, wherein the bias current control means is coupled between the first MOS transistor and the second MOS transistor to control the first and second bias voltages by using the resistance; and a refresh clock generator generating the refresh clock signal having the frequency which is controlled or adjusted based on the first and second bias voltages.